**A Very Fast and Low Power Carry Select Adder Circuit**

Abstract—

Carry Select Adder (CSA) is known to be the fastest adder among the conventional adder structures. It is used in many data processing units for realizing faster arithmetic operations. In this paper, we present an innovative CSA architecture. It employs a novel incrementer circuit in the interim stages of the CSA. Validation of the proposed design is done through design and implementation of 16, 32 and 64-bit adder circuits. Comparisons with existing conventional fast adder architectures have been made to prove its efficiency. The performance analysis shows that the proposed architecture achieves three fold advantages in terms of delay-area-power.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis